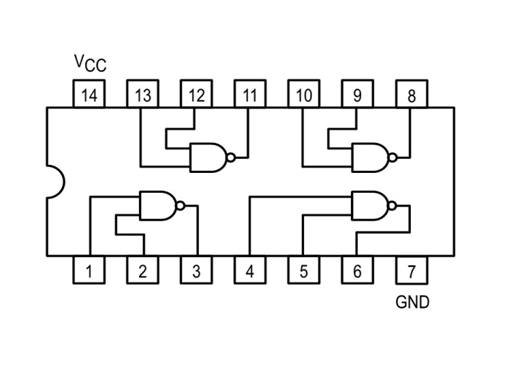
**CSCI241 – Homework #5 (Logic Gates)  
Riley Primeau**

**74LS00 – Quad 2-input NAND Gate  
Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **HIGH, 5.10 v** |
| **LOW** | **HIGH** | **HIGH, 4.27 v** |
| **HIGH** | **LOW** | **HIGH, 4.35 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **HIGH, 5.11 v** |
| **LOW** | **HIGH** | **HIGH, 4.30 v** |
| **HIGH** | **LOW** | **HIGH, 4.30 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #3**

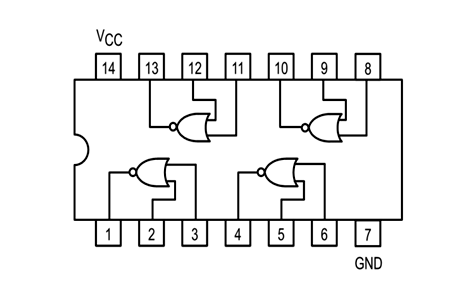
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 10)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **HIGH, 5.09 v** |
| **LOW** | **HIGH** | **HIGH, 4.28 v** |
| **HIGH** | **LOW** | **HIGH, 4.37 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **HIGH, 5.10 v** |
| **LOW** | **HIGH** | **HIGH, 4.30 v** |
| **HIGH** | **LOW** | **HIGH, 4.30 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**74LS02 – Quad 2-input NOR Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 2)** | **Input B (Pin 3)** | **Output Y (Pin 1)** |
| **LOW** | **LOW** | **HIGH, 5.10 v** |
| **LOW** | **HIGH** | **LOW, 0.17 v** |
| **HIGH** | **LOW** | **LOW, 0.01 v** |
| **HIGH** | **HIGH** | **LOW, 0.13 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 5)** | **Input B (Pin 6)** | **Output Y (Pin 4)** |
| **LOW** | **LOW** | **HIGH, 5.08 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #3**

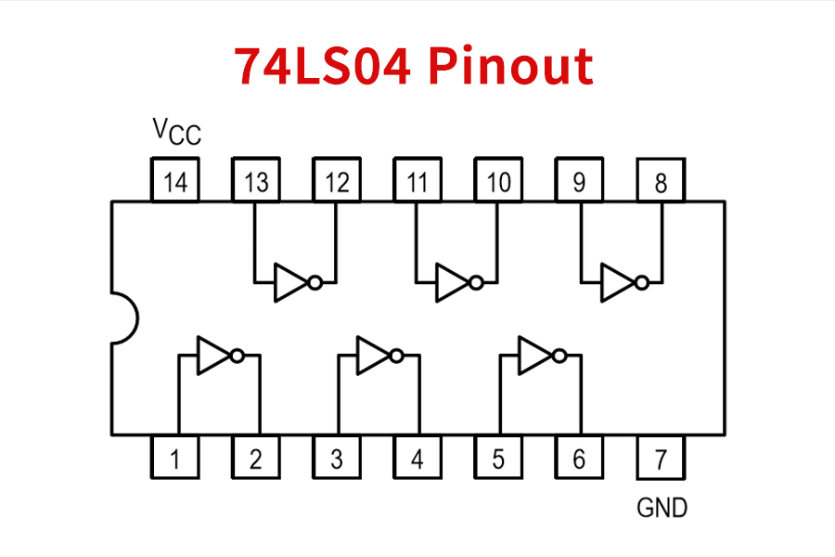
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 8)** | **Input B (Pin 9)** | **Output Y (Pin 10)** |
| **LOW** | **LOW** | **HIGH, 5.06 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **HIGH, 5.07 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**74LS04 – Hex Inverters**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |
| --- | --- |
| **Input A (Pin 1)** | **Output Y (Pin 2)** |
| **LOW** | **HIGH, 5.11** |
| **HIGH** | **LOW, 0.00 v** |

**Gate #2**

|  |  |
| --- | --- |
| **Input A (Pin 3)** | **Output Y (Pin 4)** |
| **LOW** | **HIGH, 5.09** |
| **HIGH** | **LOW, 0.00 v** |

**Gate #3**

|  |  |
| --- | --- |
| **Input A (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **HIGH, 5.11** |
| **HIGH** | **LOW, 0.00 v** |

**Gate #4**

|  |  |
| --- | --- |
| **Input A (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **HIGH, 5.08** |
| **HIGH** | **LOW, 0.00 v** |

**Gate #5**

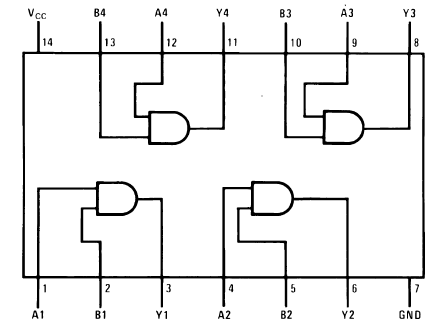
|  |  |
| --- | --- |
| **Input A (Pin 11)** | **Output Y (Pin 10)** |
| **LOW** | **HIGH,** |
| **HIGH** | **LOW, 0.00 v** |

**Gate #6**

|  |  |
| --- | --- |
| **Input A (Pin 13)** | **Output Y (Pin 12)** |
| **LOW** | **HIGH,** |
| **HIGH** | **LOW, 0.00 v** |

**74LS08 – Quad 2-input AND Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 5.12 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 5.10 v** |

**Gate #3**

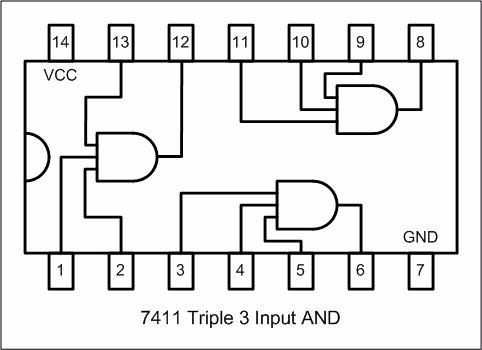
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 10)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 5.08 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 5.10 v** |

**74LS11 – Triple 3-input AND Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Input C (Pin 13)** | **Output Y (Pin 12)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**Gate #2**

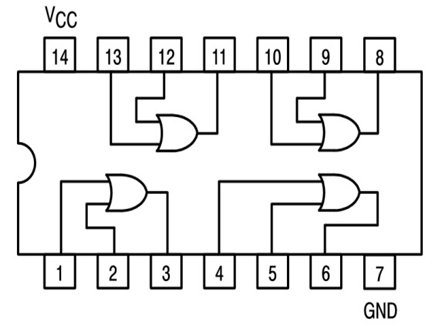
|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 3)** | **Input B (Pin 4)** | **Input C (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.09 v** |

**Gate #3**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 11)** | **Input B (Pin 10)** | **Input C (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**74LS32 – Quad 2-input OR Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**Gate #3**

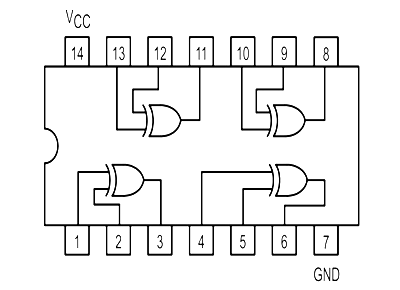
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 10)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **HIGH, 5.11 v** |

**74LS86 – Quad 2-input XOR Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.09 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.10 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 10)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.11 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.08 v** |
| **HIGH** | **HIGH** | **LOW, 0.00 v** |

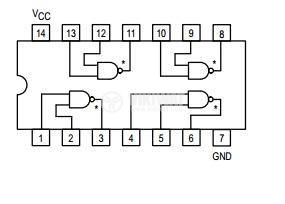
**74LS03 – Quad 2-input NAND Gate with Open Collector Outputs**

**Test Circuit: Pin1 – HIGH, Pin 2 – HIGH**

**Diagram

Description automatically generated**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y** |
| **LOW** | **LOW** | **HIGH, 5.11v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.10 v** |
| **HIGH** | **HIGH** | **LOW, 0.49 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y** |
| **LOW** | **LOW** | **HIGH, 5.10v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.10 v** |
| **HIGH** | **HIGH** | **LOW, 0.49 v** |

**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y** |
| **LOW** | **LOW** | **HIGH, 5.09v** |
| **LOW** | **HIGH** | **HIGH, 5.10 v** |
| **HIGH** | **LOW** | **HIGH, 5.11 v** |
| **HIGH** | **HIGH** | **LOW, 0.49 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y** |
| **LOW** | **LOW** | **HIGH, 5.11v** |
| **LOW** | **HIGH** | **HIGH, 5.09 v** |
| **HIGH** | **LOW** | **HIGH, 5.09 v** |
| **HIGH** | **HIGH** | **LOW, 0.49 v** |